
Taming Analog Model Complexity

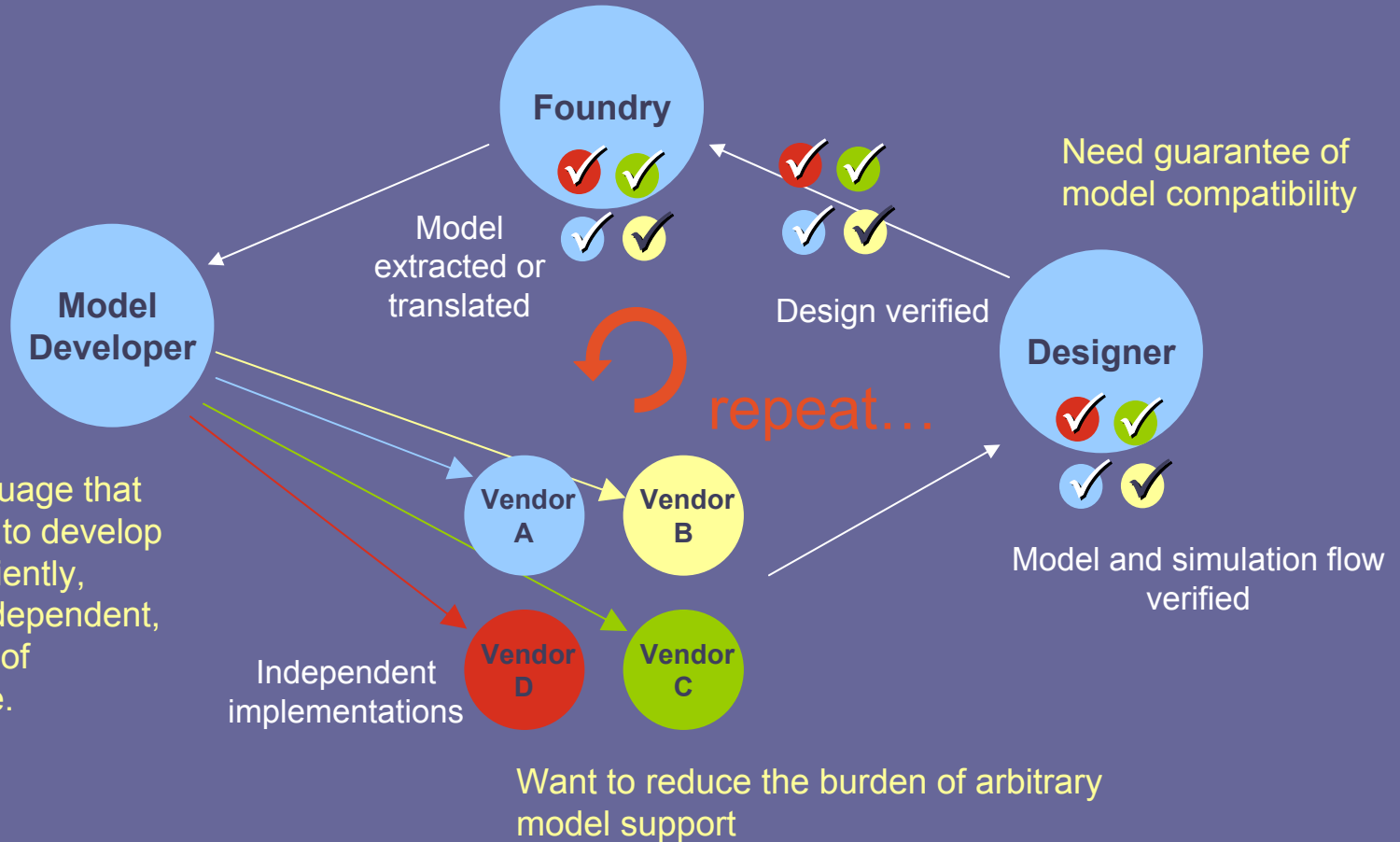
Marek Mierzwinski

Tiburon Design Automation, Inc.

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Typical model flow

Want to support 1 parameter set



Model Implementation Issues

Existing source-code interfaces pose challenges

- Inherently non-portable
- High burden on the developer to:
 - Manually compute matrix stamp
 - Manually compute derivatives
 - Implement multiple, self-consistent entry points for analysis types
 - Be familiar with simulator-specific architecture
- Require close cooperation with the simulator vendor
 - Timely updates and defect fixes are difficult

Existing solution

Current analog-HDL simulators are

- Slow
- Not universally available
- Do not offer IP protection

For analog modeling

- Speed equivalent to simulator built-ins
- Support of a wide range of analysis types (including RF)
 - Support for noise, sensitivity analysis, optimization, and efficient sweeping.
- Language must be supported consistently
- Model validation, checking, and debugging tools are critical

Tiburon Design Automation Solution

A Next-Generation Verilog-A compiler technology deployed across all major analog simulation platforms.

- Performance and robustness rivaling that of existing C/C++ level interfaces.
- Support all analysis types, e.g. transient, harmonic balance, shooting.
- Models to be developed once and run everywhere.

Verilog-A Solution

For the vendor

- Removes need to support complicated standard models.
- Proprietary Verilog-A models still can be developed.

For the foundry

- One parameter set.

For the end-user

- Solves the problem of model implementation and compatibility.

For the model developer

- Concentrate on model, not simulator issues.
- Immediately available on all platforms.

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